What is claimed is:

1. A method for writing to a memory array, the method comprising:

(a) providing a memory array comprising a primary block of memory cells and a redundant block of memory cells; and

(b) in response to an error in writing to the primary block:

(b1) storing a flag in a set of memory cells allocated to the primary block; and

(b2) writing to the redundant block.

2. The invention of Claim 1 further comprising:

(c) in response to a command to read the primary block, reading the set of memory cells allocated to the primary block; and

(d) in response to reading the flag stored in the set of memory cells, reading the redundant block.

3. The invention of Claim 1, wherein the primary block comprises a plurality of smaller blocks, and wherein the error in writing to the primary block occurs when there is an error in writing at least one bit in one of the smaller blocks.

4. The invention of Claim 3, wherein the smaller block comprises an oct-byte and the primary block comprises a page.

5. The invention of Claim 1, wherein the error occurs when there is an error in writing a single bit.

6. The invention of Claim 1, wherein the error occurs when there is an error in writing two bits.

7. The invention of Claim 1, wherein the error occurs when there is an error in writing X bits, wherein X is sufficient to introduce an error that is uncorrectable by an error protection scheme protecting at least some of the memory cells in the primary block.

8. The invention of Claim 1 further comprising determining the error occurred by:

attempting to program a memory cell in the primary block; and

while attempting to program the memory cell, determining that the memory cell is not in a programmed state.

9. The invention of Claim 1 further comprising determining the error occurred by:

attempting to program a memory cell in the primary block;

reading the memory cell after the attempt to program the memory cell; and

determining that the memory cell is not in a programmed state.

10. The invention of Claim 1, wherein the primary block is associated with the redundant block via direct mapping.

11. The invention of Claim 1, wherein the primary block is associated with the redundant block via set-associative mapping.

12. The invention of Claim 1, wherein the primary block is associated with the redundant block via fully-associative mapping.

13. The invention of Claim 1, wherein the memory array comprises write-once memory cells.

14. The invention of Claim 1, wherein the memory array comprises a three-dimensional memory array of vertically-stacked field-programmable memory cells.

15. The invention of Claim 1, wherein the memory array comprises a semiconductor material.

16. The invention of Claim 1, wherein (b) is performed by a memory device comprising the memory array.

17. The invention of Claim 1, wherein (b) is performed by a host device coupled with a memory device comprising the memory array.

18. A method for writing to a memory array, the method comprising:

(a) providing a memory array comprising a primary block of memory cells and a redundant block of memory cells;

(b) attempting to write to the primary block;

(c) while attempting to write to the primary block, determining that an error occurred in writing to the primary block; and

(d) writing to the redundant block.

19. The invention of Claim 18 further comprising:

storing a flag in a set of memory cells allocated to the primary block in response to the error in writing to the primary block.

20. The invention of Claim 19, wherein the flag is stored by a memory device comprising the memory array.

21. The invention of Claim 19, wherein the flag is stored by a host device coupled with a memory device comprising the memory array.

22. The invention of Claim 19 further comprising:

in response to a command to read the primary block, reading the set of memory cells allocated to the primary block; and

in response to reading the flag stored in the set of memory cells, reading the redundant block.

23. The invention of Claim 18, wherein the primary block is associated with the redundant block via direct mapping.

24. The invention of Claim 18, wherein the primary block is associated with the redundant block via set-associative mapping.

25. The invention of Claim 18, wherein the primary block is associated with the redundant block via fully-associative mapping.

26. The invention of Claim 18 further comprising:

storing an address of the primary block in a redundancy address matching circuit.

27. The invention of Claim 26 further comprising in response to a command to read the primary block:

determining that the address of the primary block is stored the redundancy address matching circuit; and

reading the redundant block.

28. The invention of Claim 18, wherein the primary block comprises a plurality of smaller blocks, and wherein the error in writing to the primary block occurs when there is an error in writing at least one bit in one of the smaller blocks.

29. The invention of Claim 28, wherein the smaller block comprises an oct-byte and the primary block comprises a page.

30. The invention of Claim 18, wherein the error occurs when there is an error in writing a single bit.

31. The invention of Claim 18, wherein the error occurs when there is an error in writing two bits.

32. The invention of Claim 18, wherein the error occurs when there is an error in writing X bits, wherein X is sufficient to introduce an error that is uncorrectable by an error protection scheme protecting at least some of the memory cells in the primary block.

33. The invention of Claim 18, wherein the memory array comprises write-once memory cells.

34. The invention of Claim 18, wherein the memory array comprises a three-dimensional memory array of vertically-stacked field-programmable memory cells.

35. The invention of Claim 18, wherein the memory array comprises a semiconductor material.

36. A memory device comprising:

a three-dimensional memory array of vertically-stacked field-programmable memory cells, the memory array comprising a primary block of memory cells and a redundant block of memory cells; and

redundancy circuitry operative to write to the redundant block in response to an error in writing to the primary block.

37. The invention of Claim 36, wherein the redundancy circuitry is operative to, in response to an error in writing to the primary block, store a flag in a set of memory cells allocated to the primary block.

38. The invention of Claim 37, wherein the redundancy circuitry is further operative to, in response to a command to read the primary block, read the set of memory cells

allocated to the primary block; and, in response to reading the flag stored in the set of memory cells, read the redundant block.

39. The invention of Claim 37, wherein the redundancy circuitry comprises a redundancy address matching circuit.

40. The invention of Claim 36 further comprising write circuitry operative to attempt to program a memory cell in the primary block and, while attempting to program the memory cell, determine that the error occurred in writing to the primary block.

41. The invention of Claim 36 further comprising write circuitry operative to attempt to program a memory cell in the primary block, read the memory cell after the attempt to program the memory cell, and determine that the error occurred in writing to the primary block.

42. The invention of Claim 36, wherein the memory array comprises write-once memory cells.

43. The invention of Claim 36, wherein the memory array comprises a semiconductor material.

44. A method for testing a memory array, the method comprising:

(a) providing a memory array comprising a primary block of memory cells and a redundant block of memory cells, wherein the primary block comprises a set of memory cells allocated for writing test bits;

(b) in response to an error in writing test bits in the primary block, storing a flag in a set of memory cells allocated to the primary block;

(c) in response to a command to write to the primary block, reading the set of memory cells allocated to the primary block; and

(d) in response to reading the flag stored in the set of memory cells, writing to the redundant block.

45. The invention of Claim 44, wherein the memory array comprises write-once memory cells.

46. The invention of Claim 44, wherein the memory array comprises a three-dimensional memory array of vertically-stacked field-programmable memory cells.

47. The invention of Claim 44, wherein the memory array comprises a semiconductor material.